Distributed Operating Systems

Side-Channels

Marcus Hähnel (marcus.haehnel@kernkonzept.com)

2023-07-03

2023-07-04

DOS - Side-Channels

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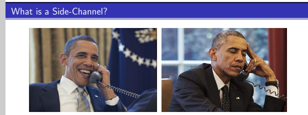
What is a Side-Channel?



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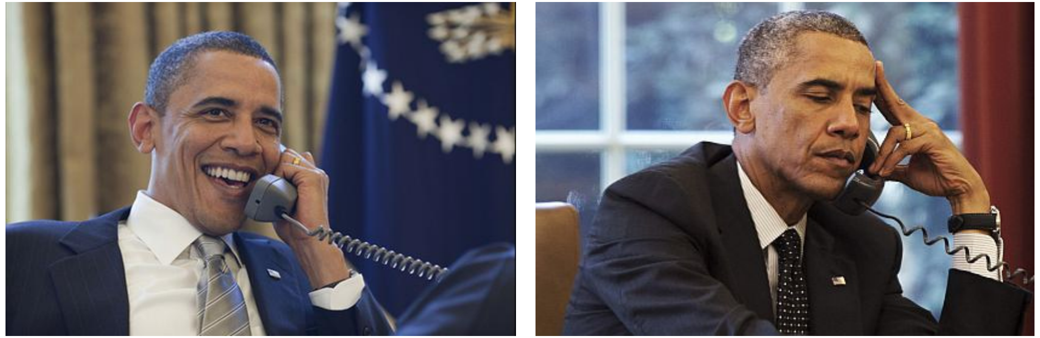


Visual side-channel

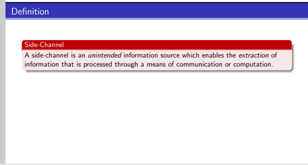
Which call has a positive connotation?

What is a Side-Channel?
Visual side-channel
Which call has a positive connotation?

Definition

Side-Channel

A side-channel is an *unintended* information source which enables the *extraction* of information that is processed through a means of communication or computation.



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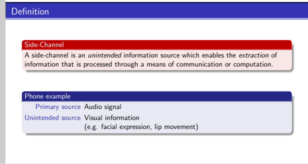
Phone example

Primary source	Audio signal
Unintended source	Visual information (e.g. facial expression, lip movement)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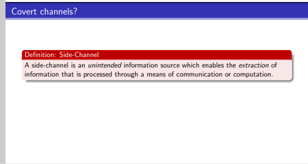
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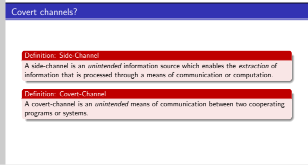
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Side-Channel usage

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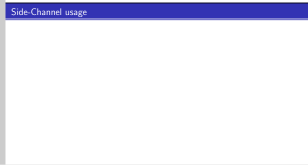
└Introduction

└Side-Channel usage

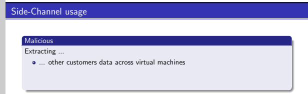

Side-Channel usage

Side-Channel usage

Malicious

Extracting ...

- ... other customers data across virtual machines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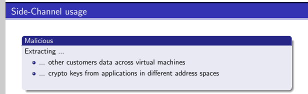
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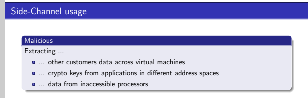
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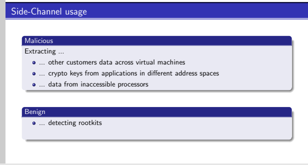
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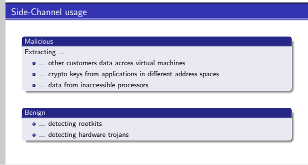
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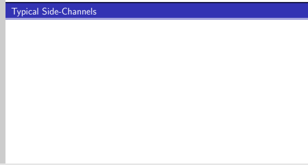
Typical Side-Channels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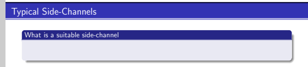

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What is a suitable side-channel

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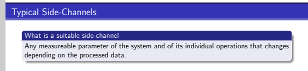
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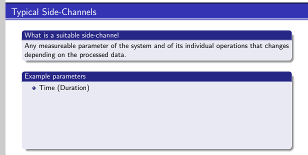
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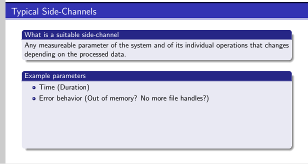
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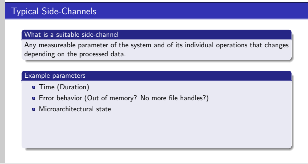
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DOS - Side-Channels
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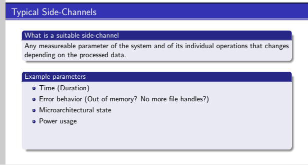

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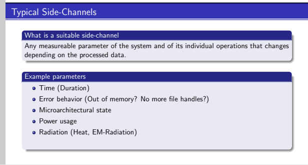
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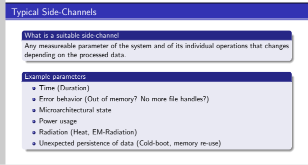
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Timing Channels

Attack vector

The duration of an attacker observable operation depends on the data processed by the victim

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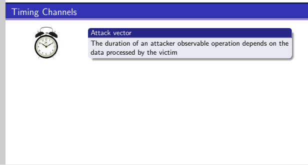
└Internal Attack Vectors
└Timing Channels
└Timing Channels



Timing Channels

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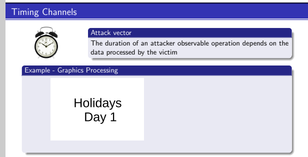
Example - Graphics Processing



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Example - Graphics Processing

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DOS - Side-Channels
└Internal Attack Vectors
 └Timing Channels
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Timing Channels

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Example - Graphics Processing

Holidays
Day 1

Convert to png: 1 s vs. 17 s

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DOS - Side-Channels
└Internal Attack Vectors
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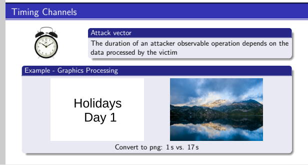

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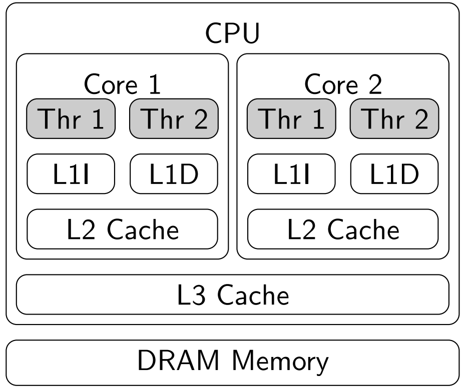
Cache Side-Channel



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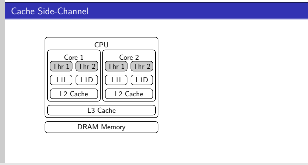

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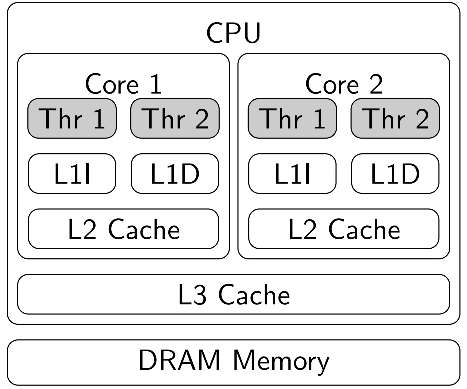

Level	Size	Cycles
L1D	32 KiB	4
L1I	32 KiB	4
L2	256 KiB	12
L3	3 MiB	36
DRAM	large	250

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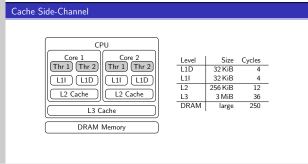
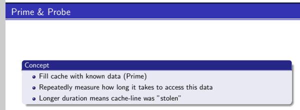


Prime & Probe

Concept

- Fill cache with known data (Prime)
- Repeatedly measure how long it takes to access this data
- Longer duration means cache-line was "stolen"



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Example (Victim)

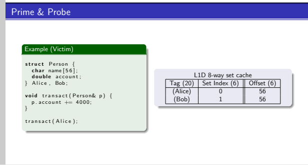
```
struct Person {
  char name[56];
  double account;
} Alice, Bob;

void transact(Person& p) {
  p.account += 4000;
}

transact(Alice);
```

L1D 8-way set cache

Tag (20)	Set Index (6)	Offset (6)
(Alice)	0	56
(Bob)	1	56



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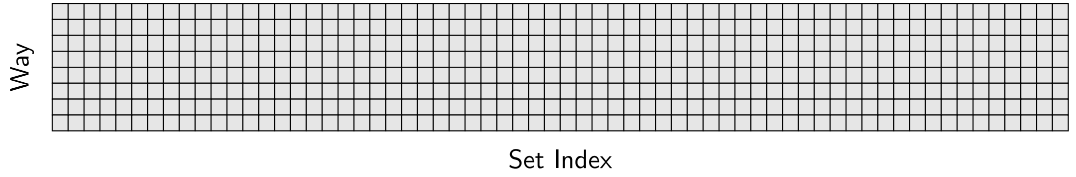

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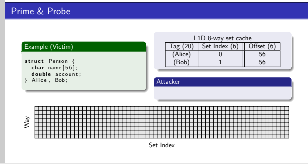

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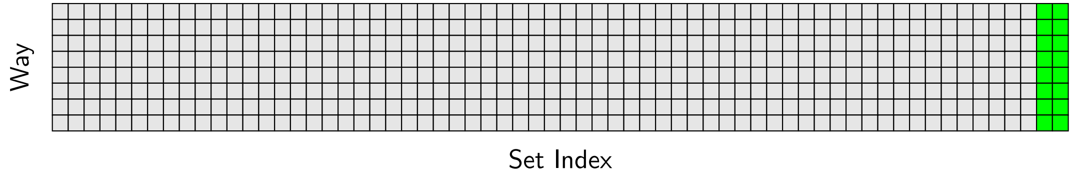

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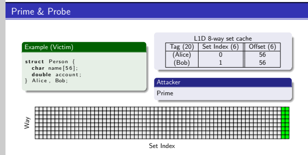

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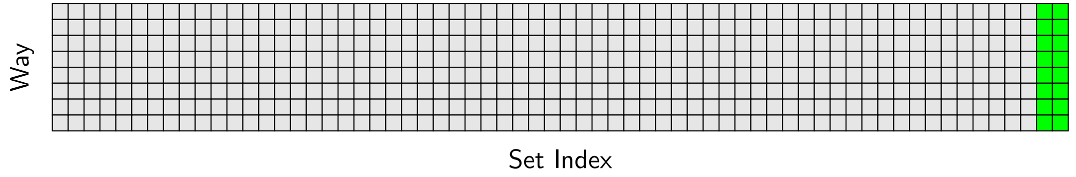

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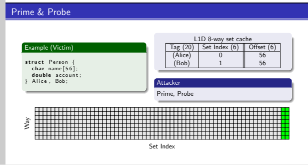
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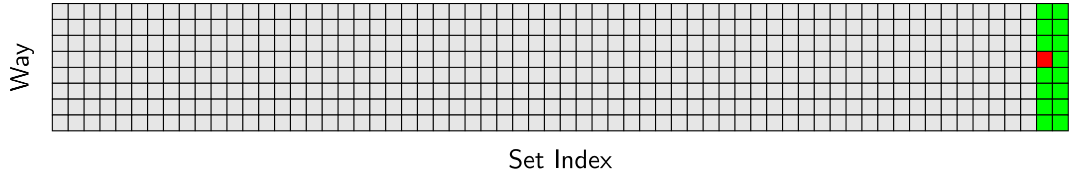
Attacker

Prime, Probe, Detect



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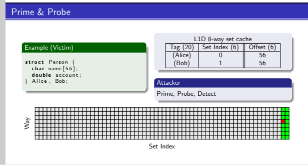

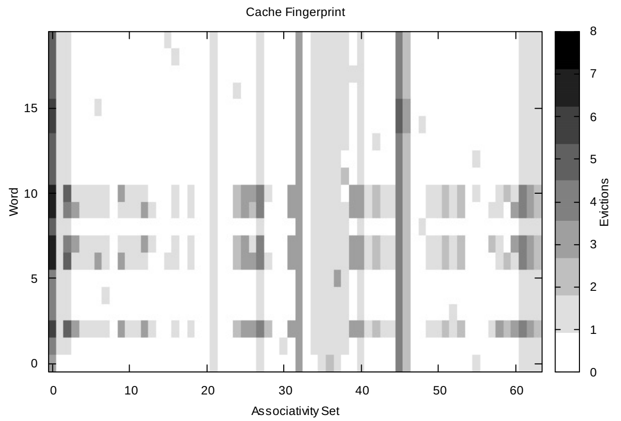

Results of prime-probe observations for 20 distinct processed text words (rows). Darker fields indicate more evicted ways within an 8-way associativity set. Vertical lines identify cache addresses evicted in every observation.

DOS - Side-Channels
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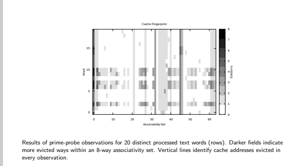
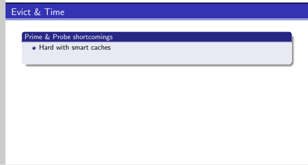


Evict & Time

Prime & Probe shortcomings

- Hard with smart caches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Evict & Time

Prime & Probe shortcomings

- Hard with smart caches
- Probing is prone to many false positives

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DOS - Side-Channels
└Internal Attack Vectors
└Timing Channels
└Evict & Time

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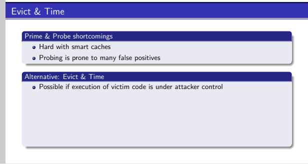
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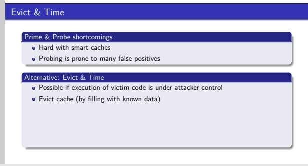
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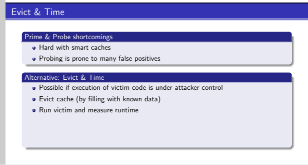
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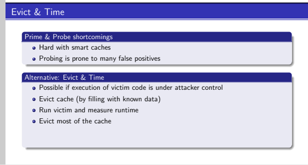
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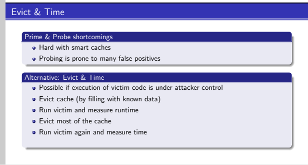

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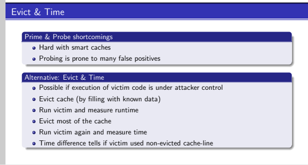
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Smart Caches

Smart Caches "reserve" parts of the L3 cache for individual cores. This makes priming hard.

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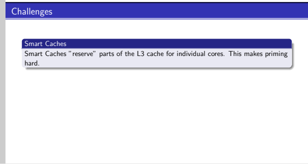
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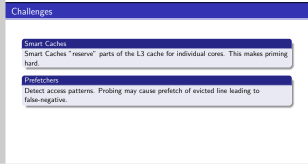

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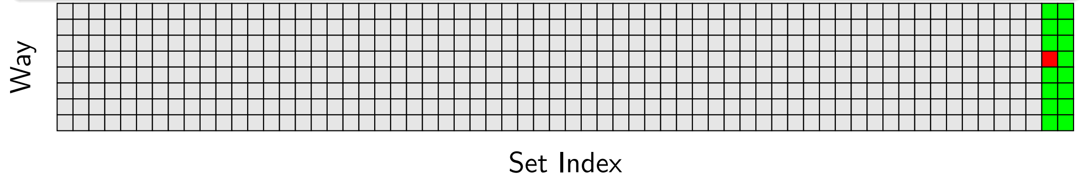

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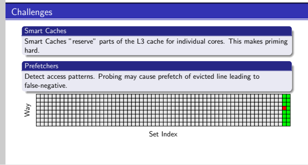

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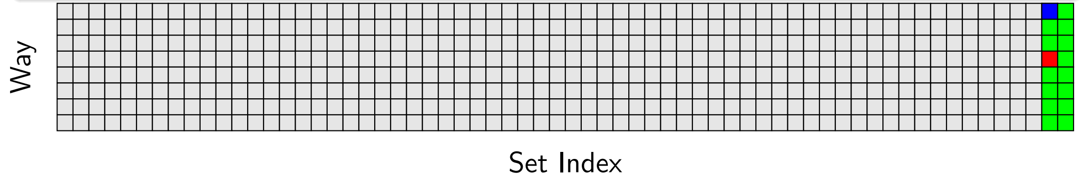

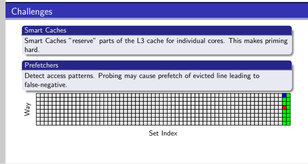
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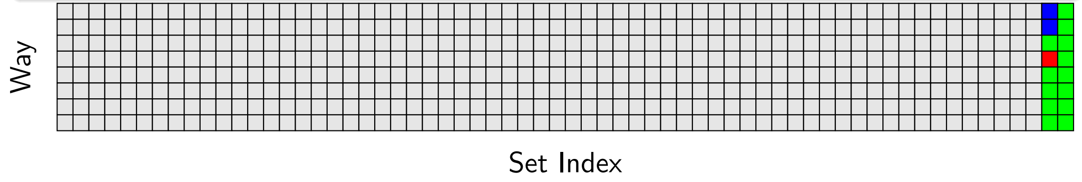

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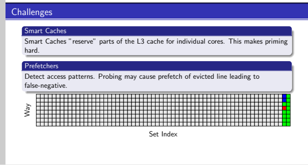

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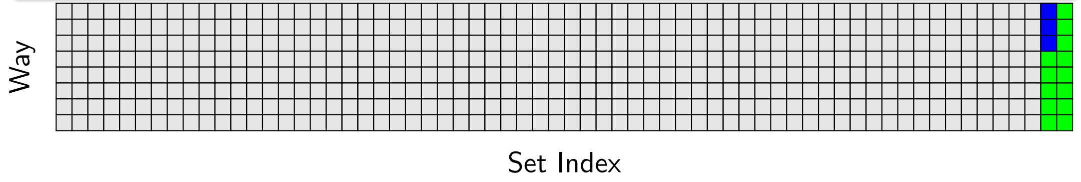

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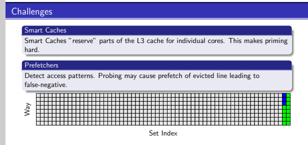

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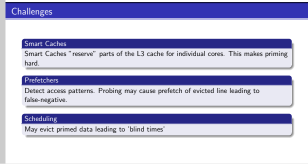
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Pagefault Side-Channel

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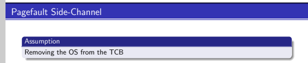
Removing the OS from the TCB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Scenario: Shielding Systems

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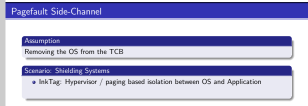
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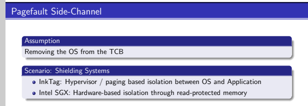
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Vulnerability

- These systems don't trust OS but use it to configure hardware
- OS makes a powerful adversary

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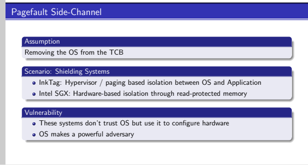
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First attack vector against Intel SGX

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System Model

- OS cannot directly observe memory or registers of application
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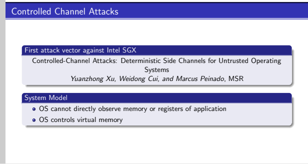
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Example (Source, simplified)

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//str on heap
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- Heap not present

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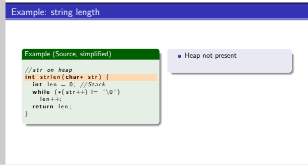
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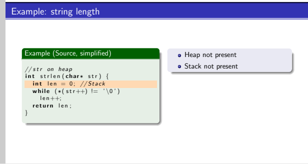
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	Phys-Addr	other Flags	P
Heap	...	...	0
Stack	...	...	0

Attackers Knowledge

Length = 0

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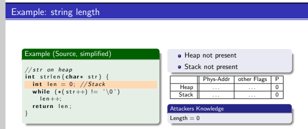
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! Heap	...	...	0
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2023-07-04

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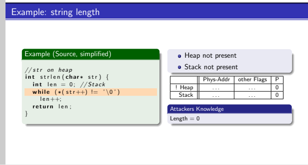
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- Heap not present
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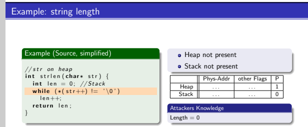
	Phys-Addr	other Flags	P
Heap	...	...	1
Stack	...	...	0

Attackers Knowledge

Length = 0



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Attackers Knowledge

Length = 1

2023-07-04

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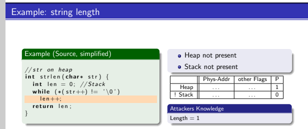
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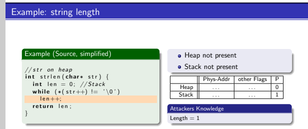
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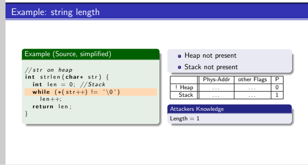
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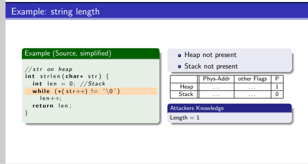
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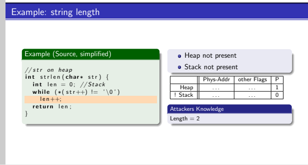
	Phys-Addr	other Flags	P
Heap	...	...	1
! Stack	...	...	0

Attackers Knowledge

Length = 2

2023-07-04

DOS - Side-Channels
└Internal Attack Vectors
  └Fault Channels
    └Example: string length


Example: string length

Example (Source, simplified)

```
//str on heap
int strlen(char* str) {
  int len = 0; //Stack
  while (*(str++) != '\0')
    len++;
  return len;
}
```

- Heap not present
- Stack not present

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Heap	...	...	1
! Stack	...	...	0

Attackers Knowledge

Length = 2

Example: string length

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Attackers Knowledge

Length = 2

2023-07-04

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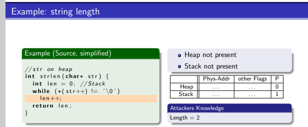
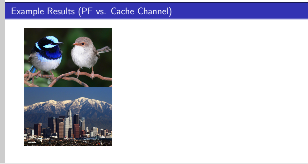
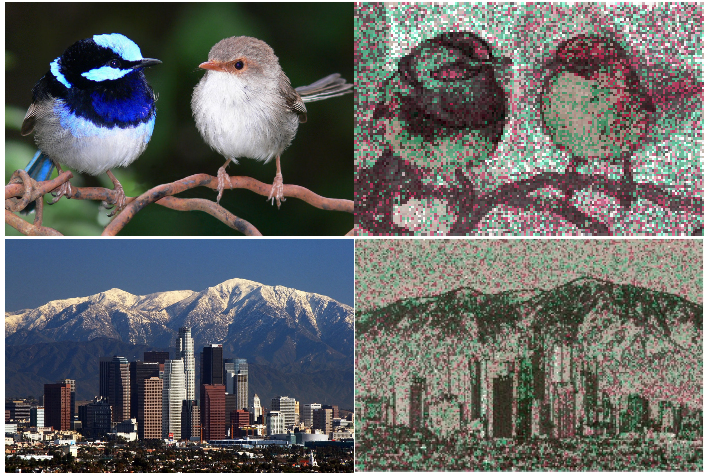


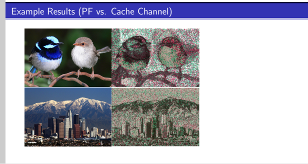
Example Results (PF vs. Cache Channel)



1. IDCT (inverse discrete cosine transformation)
2. Index in array ≈8 kB big

Example Results (PF vs. Cache Channel)





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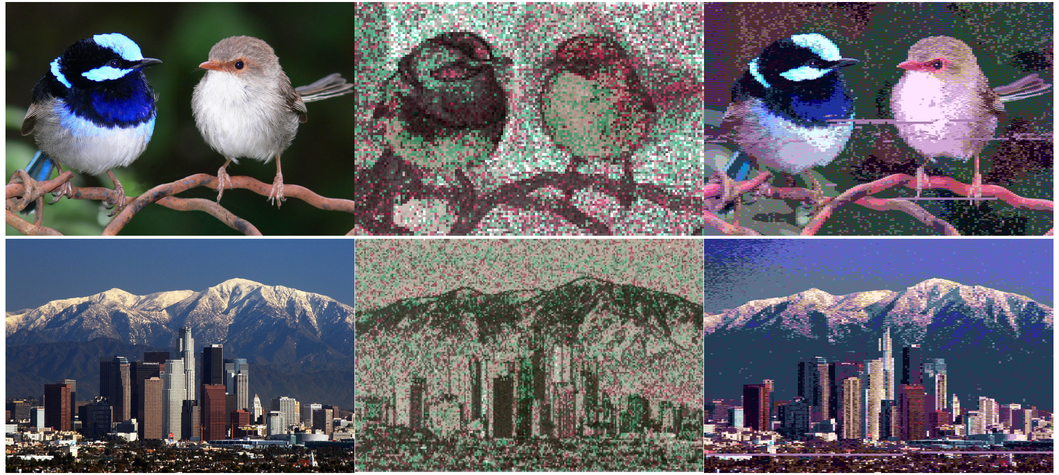

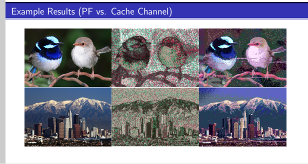

1. IDCT (inverse discrete cosine transformation)
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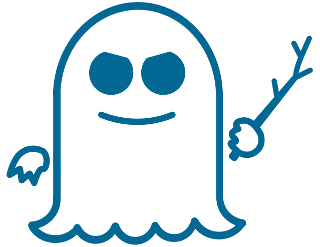
Microarchitectural Channels

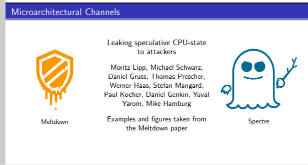
Meltdown

Leaking speculative CPU-state to attackers

Moritz Lipp, Michael Schwarz, Daniel Gruss, Thomas Prescher, Werner Haas, Stefan Mangard, Paul Kocher, Daniel Genkin, Yuval Yarom, Mike Hamburg

Examples and figures taken from the Meltdown paper


Spectre



Side-Effects of Out-of-Order execution

Toy Example

```
raise_exception();
// the line below is never reached
access(probe_array[data*4096]);
```

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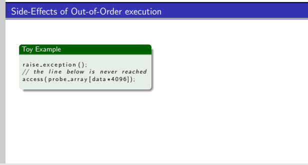
DOS - Side-Channels
└Internal Attack Vectors
  └Microarchitectural Channels
    └Side-Effects of Out-of-Order execution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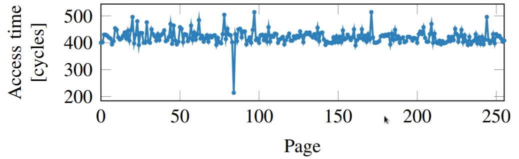

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DOS - Side-Channels
└Internal Attack Vectors
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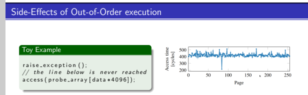

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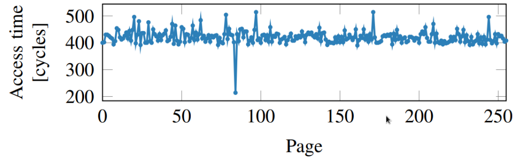

Constraints

- Raising the exception should be slow
- Accessing the array should be fast

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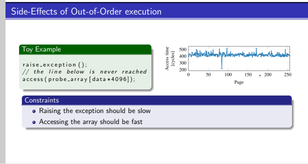
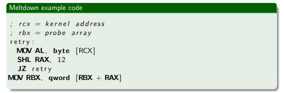
DOS - Side-Channels
└Internal Attack Vectors
  └Microarchitectural Channels
    └Side-Effects of Out-of-Order execution



Meltdown example code

```
; rcx = kernel address
; rbx = probe array
retry:
  MOV AL, byte [RCX]
  SHL RAX, 12
  JZ retry
MOV RBX, qword [RBX + RAX]
```



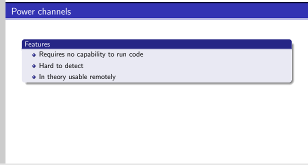
1. Retry needed because execption handling zeroes registers
2. No evicted cache line is considered zero
3. Exception can be prevented (amongst others) using TSX

Power channels

Features

- Requires no capability to run code
- Hard to detect
- In theory usable remotely

DOS - Side-Channels
└External Attack Vectors
  └Power channels
    └Power channels



Power channels

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Power channels

Features

- Requires no capability to run code
- Hard to detect
- In theory usable remotely

Requirements

- (very) high-resolution power measurement
- physical access to power supply
- detailed knowledge about exact processor used

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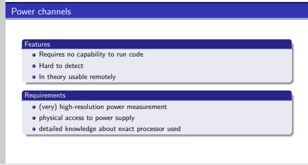
DOS - Side-Channels
└External Attack Vectors
 └Power channels
  └Power channels



Example

Example (Square-And-Multiply)

```
int exp(int base, int e) {
  int res = 1;
  while (e != 0) {
    res *= res; //square
    if (e & 1) res *= base; //multiply
    e >>= 1;
  }
  return res;
}
```

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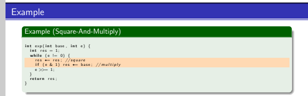
DOS - Side-Channels
└External Attack Vectors
  └Power channels
    └Example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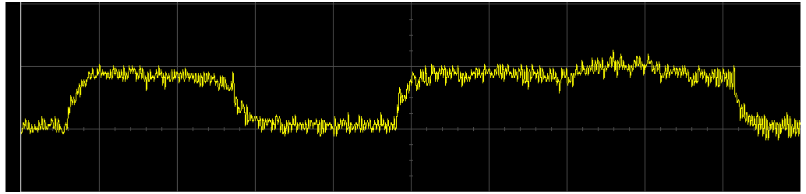
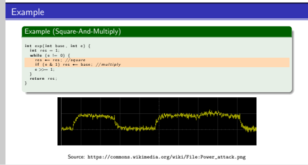


Source: https://commons.wikimedia.org/wiki/File:Power_attack.png

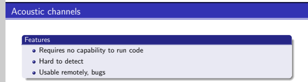
DOS - Side-Channels
└External Attack Vectors
  └Power channels
    └Example



Acoustic channels

Features

- Requires no capability to run code
- Hard to detect
- Usable remotely, bugs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Acoustic channels

Features

- Requires no capability to run code
- Hard to detect
- Usable remotely, bugs

Requirements

- Good audio equipment
- Reliable audio filters
- Knowledge about typing style
- Knowledge about hardware used

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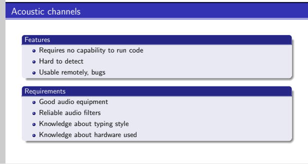
DOS - Side-Channels
└External Attack Vectors
  └Acoustic and Radiation
    └Acoustic channels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Example

Password typing attack

Keyboard Acoustic Emanations Revisited
*L*i Zhuang, Feng Zhou, J. D. Tygar
University of California, Berkeley

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DOS - Side-Channels
└External Attack Vectors
└Acoustic and Radiation
└Example

Example
Password typing attack
Keyboard Acoustic Emanations Revisited
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University of California, Berkeley

Example

Password typing attack

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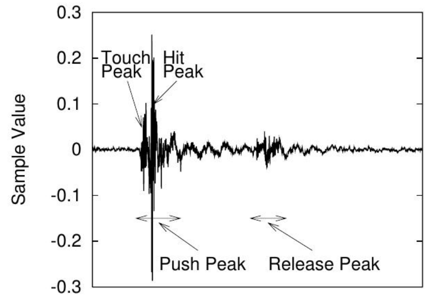

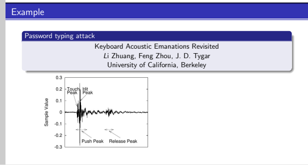

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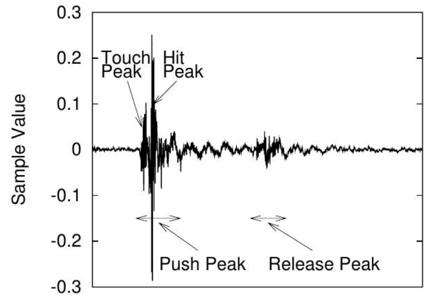

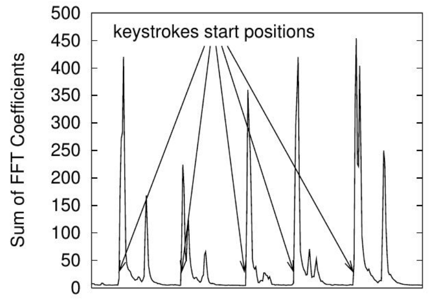

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DOS - Side-Channels
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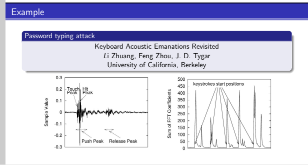
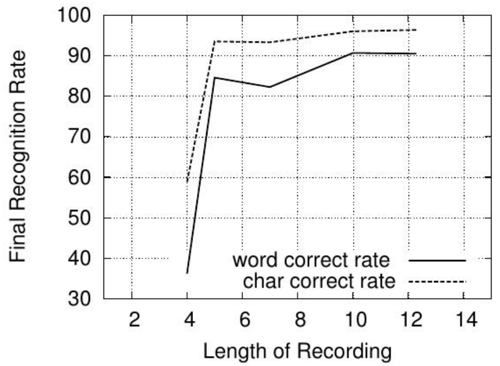
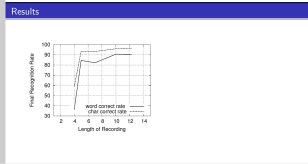
    └Example



Results


Final Recognition Rate
Length of Recording
word correct rate
char correct rate



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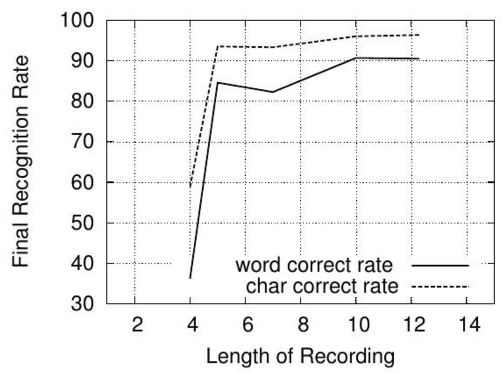
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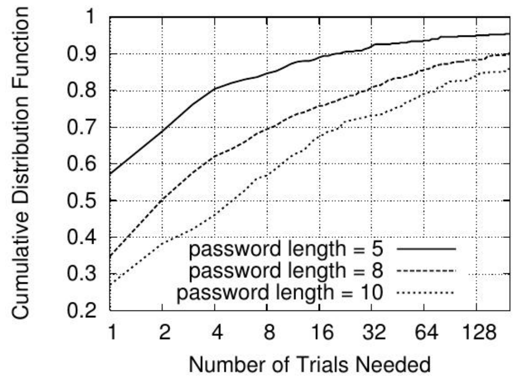
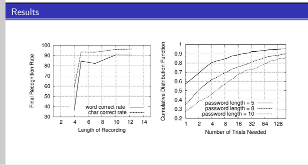

Cumulative Distribution Function
Number of Trials Needed
password length = 5
password length = 8
password length = 10



Electro Magnetic (EM) Radiation

Features

- Requires no capability to run code
- Hard to detect
- No "wire-cutting" needed

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DOS - Side-Channels
└External Attack Vectors
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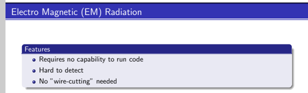
    └Electro Magnetic (EM) Radiation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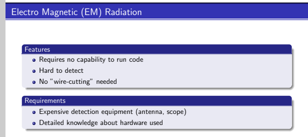
Requirements

- Expensive detection equipment (antenna, scope)
- Detailed knowledge about hardware used



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Data Remanence

Warning

- NOT a classical side-channel
- no indirect observance of data → direct

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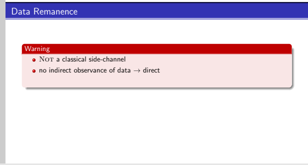
DOS - Side-Channels
└Data remanence
└Data Remanence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Data Remanence

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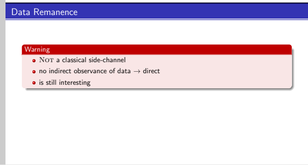

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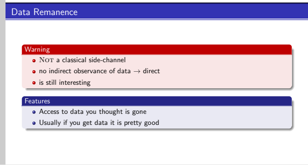
Features

- Access to data you thought is gone
- Usually if you get data it is pretty good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Examples / Software

Example (Your friend, the compiler)

```
void secret() {
  char* buf = (char*)malloc(1024);
  // put sth. secret into buf

  free(buf);
}
```

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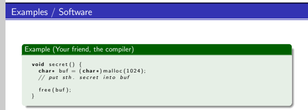
DOS - Side-Channels
└Data remanence
  └Software
    └Examples / Software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?

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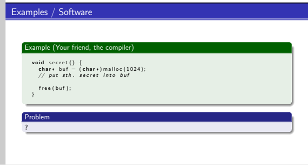
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Examples / Software

Example (Your friend, the compiler)

```
void secret() {
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  memset(buf,'\0',1024);
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Problem

What if someone gets the same memory?

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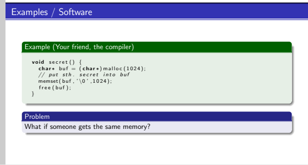
DOS - Side-Channels
└Data remanence
  └Software
    └Examples / Software



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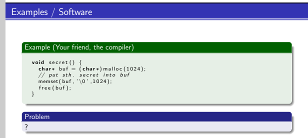

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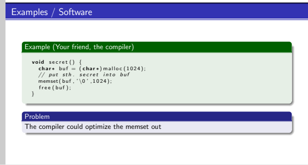
Problem

The compiler could optimize the memset out



Cold Boot

Lest We Remember: Cold Boot Attacks on Encryption Keys

J. Alex Halderman, Seth D. Schoen, Nadia Heninger, William Clarkson, William Paul, Joseph A. Calandrino , Ariel J. Feldman, Jacob Appelbaum, and Edward W. Felten
Princeton University, Electronic Frontier Foundation, Wind River Systems

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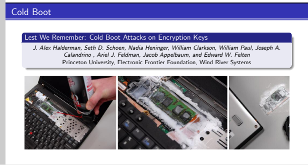
DOS - Side-Channels
└Data remanence
 └Hardware
  └Cold Boot



Cold Boot

Lest We Remember: Cold Boot Attacks on Encryption Keys

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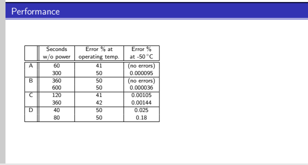
Princeton University, Electronic Frontier Foundation, Wind River Systems

Performance

	Seconds w/o power	Error % at operating temp.	Error % at -50 °C
A	60	41	(no errors)
	300	50	0.000095
B	360	50	(no errors)
	600	50	0.000036
C	120	41	0.00105
	360	42	0.00144
D	40	50	0.025
	80	50	0.18

DOS - Side-Channels
└Data remanence
└Hardware
└Performance



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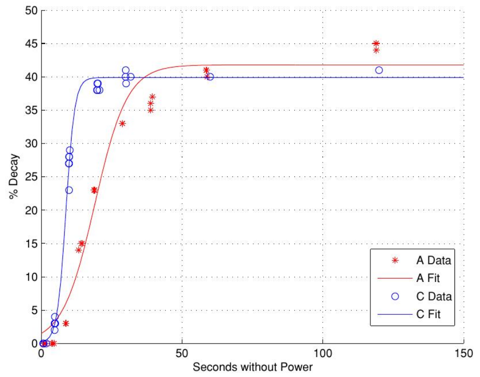

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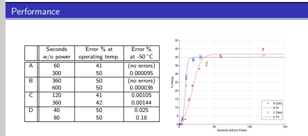

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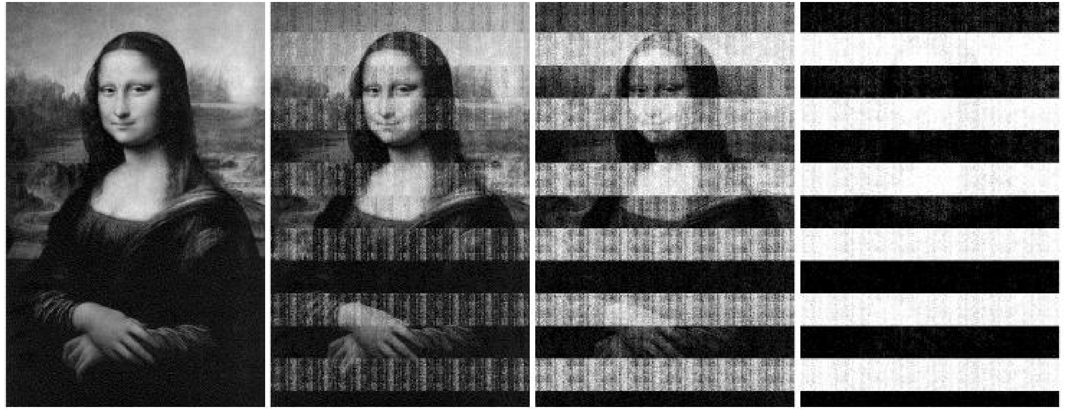
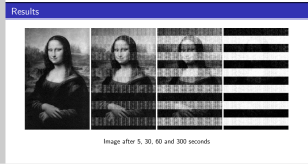


Image after 5, 30, 60 and 300 seconds



Defense mechanisms

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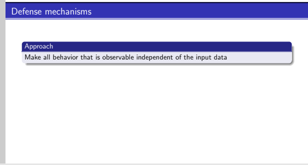
Make all behavior that is observable independent of the input data



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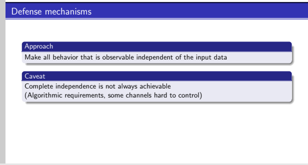
Complete independence is not always achievable
(Algorithmic requirements, some channels hard to control)



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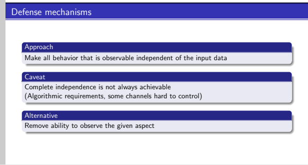
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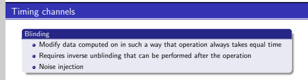
- Modify data computed on in such a way that operation always takes equal time
- Requires inverse unblinding that can be performed after the operation
- Noise injection



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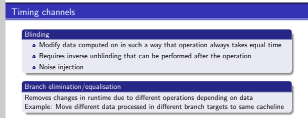
Branch elimination/equalisation

Removes changes in runtime due to different operations depending on data
Example: Move different data processed in different branch targets to same cacheline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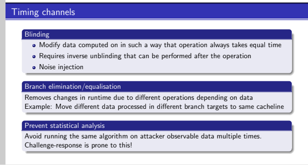
Challenge-response is prone to this!



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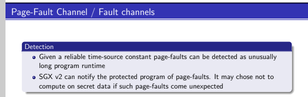
- Given a reliable time-source constant page-faults can be detected as unusually long program runtime
- SGX v2 can notify the protected program of page-faults. It may chose not to compute on secret data if such page-faults come unexpected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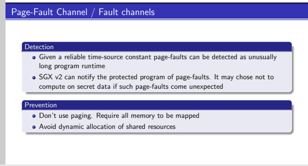

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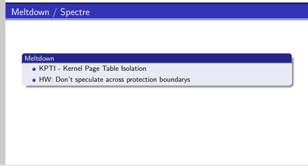
- KPTI - Kernel Page Table Isolation
- HW: Don't speculate across protection boundarys



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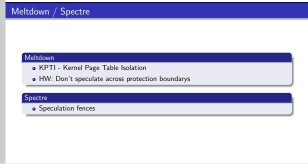
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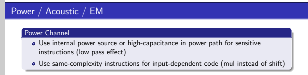
- Use internal power source or high-capacitance in power path for sensitive instructions (low pass effect)
- Use same-complexity instructions for input-dependent code (mul instead of shift)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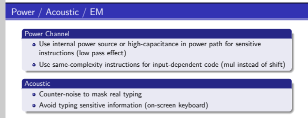
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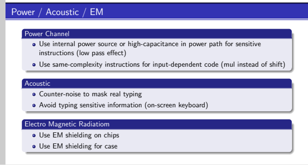
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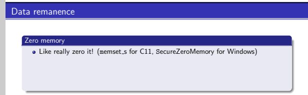
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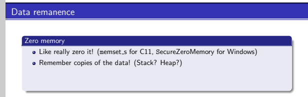
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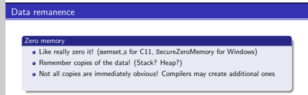
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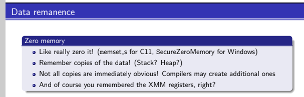
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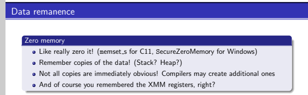
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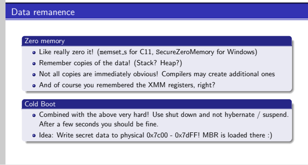
- Idea: Write secret data to physical 0x7c00 - 0x7dFF! MBR is loaded there :)



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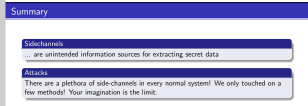
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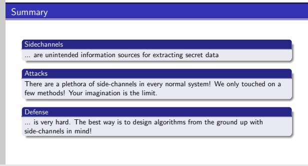

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Overview

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Cache Side-Channels

- https://www.usenix.org/system/files/conference/usenixsecurity14/sec14-paper-yarom.pdf

Page-fault Channel

- http://www.ieee-security.org/TC/SP2015/papers-archived/6949a640.pdf
- https://www.usenix.org/system/files/conference/atc17/atc17-hahnel.pdf

Microarchitectural Channels

- https://meltdownattack.com/meltdown.pdf
- https://spectreattack.com/spectre.pdf

Acoustic Channels

- http://people.eecs.berkeley.edu/ tygar/papers/Keyboard_Acoustic_Emanations_Revisited/ccs.pdf

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- http://csrc.nist.gov/groups/STM/cmvp/documents/fips140-3/physec/papers/physecpaper19.pdf
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- https://www.usenix.org/system/files/conference/atc17/atc17-hahnel.pdf
Microarchitectural Channels
- https://meltdownattack.com/meltdown.pdf
- https://spectreattack.com/spectre.pdf
Acoustic Channels
- http://people.eecs.berkeley.edu/ tygar/papers/Keyboard_Acoustic_Emanations_Revisited/ccs.pdf

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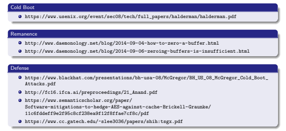
- https://www.usenix.org/event/sec08/tech/full_papers/halderman/halderman.pdf

Remanence

- http://www.daemonology.net/blog/2014-09-04-how-to-zero-a-buffer.html
- http://www.daemonology.net/blog/2014-09-06-zeroing-buffers-is-insufficient.html

Defense

- https://www.blackhat.com/presentations/bh-usa-08/McGregor/BH_US_08_McGregor_Cold_Boot_Attacks.pdf
- http://fc16.ifca.ai/preproceedings/21_Anand.pdf
- https://www.semanticscholar.org/paper/Software-mitigations-to-hedge-AES-against-cache-Brickell-Graunke/11c6fddeff9e2f95c8cf238ea9f12f8ffae7cf8c/pdf
- https://www.cc.gatech.edu/~slee3036/papers/shih:tsgx.pdf



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Defense
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- http://fc16.ifca.ai/preproceedings/21_Anand.pdf
- https://www.semanticscholar.org/paper/Software-mitigations-to-hedge-AES-against-cache-Brickell-Graunke/11c6fddeff9e2f95c8cf238ea9f12f8ffae7cf8c/pdf
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